AMENDMENTS TO THE CLAIMS:

Please amend claims 13, 15 and 23 as follows:

Claim 1 (Previously presented): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at a surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having a high power active element for radio communication formed therein, wherein said substrate, buffer layer and active layer, together form said high power semiconductor device.

Claim 2 (Previously presented): The semiconductor device as claimed in claim 1, wherein the compound semiconductor substrate has a resistivity less than 0.6×10^8 Ohm-cm.

Claim 3 (Previously presented): The semiconductor device as claimed in claim 1, wherein the active layer is formed at a position within 5.0 μm from the surface of the compound semiconductor substrate.

Claim 4 (Previously presented): The semiconductor device as claimed in claim 1, further comprising an electrode layer formed on another surface of the compound semiconductor substrate.

Claim 5 (Previously presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is not electrically connected to any power supply potential of the semiconductor device.

Claim 6 (Previously presented): The semiconductor device as claimed in claim 4, wherein the electrode layer is connected to one power supply potential of the semiconductor device.

Claim 7 (Previously presented): The semiconductor device as claimed in claim 1, further comprising:

a source electrode and a drain electrode formed on the active layer, separated from each other so as to establish a channel region, and

a gate electrode formed above the channel region.

Claim 8 (Previously presented): The semiconductor device as claimed in claim 7, wherein the active layer has 2-Dimensional Electron Gasses.

Claim 9 (canceled).

Claim 10 (Previously presented): A high power semiconductor device for a radio communication system, comprising:

a compound semiconductor substrate having a resistivity less than 1.0×10^8 Ohm-cm at least at a surface thereof;

a buffer layer formed on the compound semiconductor substrate and having a super lattice structure; and

an active layer formed on the buffer layer and having a high power active element formed therein,

wherein the compound semiconductor substrate has a resistivity of more than 1.0×10^8 Ohm-cm in total, and wherein said substrate, buffer layer and active layer, together form said high power semiconductor device.

Claim 11 (canceled).

Claim 12 (Previously presented): The semiconductor device as claimed in claim 1, wherein the buffer layer has a GaAs/A1GaAs supper lattice structure.

Claim 13 (Currently amended): The semiconductor device as claimed in claim 1, wherein the GaAs/A1GaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than 1 x [[10^5]] $\underline{10^{15}}$ cm^{-3}.

Claim 14 (Previously presented): The semiconductor device as claimed in claim 12, wherein the GaAs/A1GaAs super lattice structure includes undoped A1GaAs layers have a carrier concentration less than 1 x 10^{16} cm^{-3}.

Claim 15 (Currently amended): The semiconductor device as claimed in claim 1, wherein the active layer is doped with ~~Is~~ Si to a concentration of 1 x 10^{17} cm^{-3}.

Claim 16 (Previously presented): The semiconductor device as claimed in claim 1, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 17 (Previously presented): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is configured sufficient to inhibit electrical field concentration in the active layer upon activation of the semiconductor device.

Claim 18 (Previously presented): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is configured sufficient to inhibit accumulation, at the interface between

the low-resistance substrate layer and the buffer layer, of electrons leaking from the active layer.

Claim 19 (Previously presented): The semiconductor device as claimed in claim 1, wherein the super lattice buffer layer is configured sufficient to inhibit domain generation in the buffer layer under high power operating conditions, upon activation of the semiconductor device.

Claim 20 (Previously presented): The semiconductor device as claimed in claim 10, wherein the buffer layer has a GaAs/A1GaAs super lattice structure.

Claim 21 (Previously presented): The semiconductor device as claimed in claim 20, wherein the GaAs/A1GaAs super lattice structure includes undoped GaAs layers having a carrier concentration less than $1 \times 10^{15}\ cm^{-3}$.

Claim 22 (Previously presented): The semiconductor device as claims in claim 20, wherein the GaAs/A1GaAs super lattice structure includes undoped A1GaAs layers having a carrier concentration less than $1 \times 10^{16}\ cm^{-3}$.

Claim 23 (Currently amended): The semiconductor device as claimed in claim 10, wherein the active layer is doped with ~~Is~~ Si to a concentration of $1 \times 10^{17}\ cm^{-3}$.

Claim 24 (Previously presented): The semiconductor device as claimed in claim 10, wherein the compound semiconductor device substrate is a GaAs substrate.

Claim 25 (Previously presented): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is configured sufficient to inhibit electrical field concentration in the active layer upon activation of the semiconductor device.

Claim 26 (Previously presented): The semiconductor device as claimed in claim 10, wherein the super lattice buffer layer is configured sufficient to inhibit accumulation, at the interface between the low-resistance substrate layer and the buffer layer, of electrons leaking from the active layer.

Claim 27 (Previously presented): The semiconductor device as claimed in claim 10, wherein the super buffer layer is configured sufficient to inhibit domain generation in the buffer layer under high power operating conditions, upon activation of the semiconductor device.

Claim 28 (Previously presented): The semiconductor device as claimed in claim 10, wherein said compound semiconductor substrate comprises:

a support substrate layer having a resistivity of more than 1.0×10^8 Ohm-cm, and

a substrate surface layer provided on said support substrate layer having a resistivity of less than 1.0×10^8 Ohm-cm.